IN THE SPECIFICATION

Immediately below the paragraph ending on line 6 of page 1, and immediately above line 7 of page 1 ("Background"), add the following paragraph:

> U.S. patent application Ser. No. 08/440,101 has issued as U.S. Patents 6,026,219 and 6,505,339, entitled "Behavioral Synthesis Links to Logic synthesis," with inventors Ronald A. Miller, Donald B. MacMillen, Tai A. Ly and David W. Knapp, with issue dates, respectively, of Feb. 15, 2000 and Jan. 7, 2003.

Immediately below the last line of page 8, and before the first line of page 9, insert the text of the following 2 pages:

Figure 29 depicts template examples: (a) T1 = {(a,0) (b,1) (c,2) (d,3) (e,5) }; (b) T2 = {(f,0) (g,2) (h,5) }; (c) T3 = {(f,0) (a,1) (g,2) (b,2) (c,3) (d,4) (h,5) (e,6) }.

Figure 30 depicts an example of list scheduling failure and recovery (a) first iteration falls at T2 (b) second iteration succeeds with T1 relaxed to cstep 1.

Figure 31 shows overall flow for hierarchical scheduling.

Figure 32 shows timing constraints (a) n_j starts k cycles after n_i starts, (b) n_j starts k cycles after n_i ends and n_j has static delay d, (c) n_j starts k cycles after n_i ends and n_j's delay is not static.

Figure 33 shows models for a 3-cycle RAM write operation: (a) single node with delay = 3; (b) 3 nodes locked in a template.

Figure 34 shows template models for: (a) basic 3-stage pipelined operation, (b) 3-cycle pipelined operation with 2 stages and internal feedback, (c) 4-cycle pipelined operation with 2 stages and sequential inputs, (d) pipelined operation using a different internal path and output port.

Figure 35 shows Template Models for RAM (a) 2-cycle read, and (b) 2-cycle write.

Figure 36 shows pre-chaining examples: (a) constant with successor; (b) zero-extension with successor, (c) bit-extract with predecessor, (d) multi-input logic with predecessor or multi-output logic with successor.

Figure 37 shows handshaking for start signal: (a) original CDFG with timing constraints, (b) final CDFG scheduled.

Figure 38 shows response to an external event.

Figure. 39 shows comparison of simulation in cycle-fixed mode, where Figure 39a shows simulation of specified design (pre-synthesis) and Figure 39b shows simulation of synthesized design (post-synthesis).

Figure 40 shows loop and corresponding state graph.

Figure 41 shows loop that does not need partial unrolling.

Figure 42 shows HDL description for a multicycle addition.

Figure 43 shows two-wire handshaking protocol.

Figure 44a shows simulation before superstate-fixed scheduling; Figure 44b shows simulation after superstate-fixed scheduling.

Figure 45 shows writes to out_port_1 and out_port_2 may be permuted.

IN THE SPECIFICATION (continued)

Immediately below the last line of page 28, and before the first line of page 29, insert the text of the following 38 pages: